Surface Analysis for the Process and Device Characterisation in Microelectronics Manufacturing Plants

Rolf von Criegern, Franz Jahnel, Uwe Scheithauer, Stephen Jenkins*, Claudia Luhmann**

Siemens AG, Corporate Technology, D-81730 Munich, Germany
**(until end of 1998:) Siemens Microelectronics Ltd, PFA Department, Newcastle Upon Tyne, NE28 9NZ, United Kingdom*
***Siemens Microelectronics Center GmbH, Physical Failure Analysis, D-01099 Dresden, Germany*

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Over recent years the surface-analytical methods have been gaining importance in the analysis of structured samples from microelectronics manufacturing plants, predominantly AES (Auger Electron Spectroscopy) and dSIMS (dynamic Secondary Ion Mass Spectrometry). Complementing more conventional techniques, mainly SEM/EDX, they are widely applied to process and equipment ramp-up, process monitoring, defect identification and failure analysis. Examples of such applications are given and discussed. These methods provide vital analytical information, but the commercial instruments need further improvement in order to better meet the specialised requirements of the semiconductor manufacturing environment.

1. Introduction:

There has been an impressive advance in surface analysis techniques over the past three decades. Since microelectronic devices are made up of stacks of thin layers, whose composition, thickness and surface and interface cleanliness need to be well-defined and reproducible, there has always been a strong development and manufacturing demand for analytical methods that are able to monitor and measure these properties. The potential and actual semiconductor market demand has been a powerful driving force towards further improvements in certain aspects of commercial instrumentation and methods of data interpretation. A combination of modern surface-analytical instruments can provide almost all of the technologically relevant information on thin films and surface and interface compositions (qualitatively and semi-quantitatively) [1].

The most important surface-analytical methods to the semiconductor industry are AES (Auger Electron Spectroscopy), also termed SAM (Scanning Auger Microscopy), RBS (Rutherford Backscattering Spectroscopy), XPS (X-ray Photoelectron Spectroscopy), dynamic SIMS (Secondary Ion Mass Spectroscopy), and more recently ToF-SIMS (Time-of-Flight SIMS). For all these methods to yield their ultimate spatial resolution, depth resolution and reproducible quantification, the samples need to be flat, smooth and must have sufficiently large laterally uniform areas for the measurement. However, despite the rapid dimensional shrinkage of integrated circuits, surface analysis techniques have increasingly and successfully also been applied to real device issues. Even though topographic features and structures can complicate data interpretation, this does not exclude the possibility of reliable analysis. This will be demonstrated with a number of examples.

2. Analytical methods used in PFA sections

Optical microscopy and SEM (Scanning Electron Microscopy) with EDX analysis (energy-dispersive X-ray analysis) are the main tools applied in the physical failure analysis (PFA) departments of wafer fabs. Besides the conventional chemical and physical (cleaving or polishing) methods for sample preparation, FIB

(Focused Ion Beam) instruments have become a valuable tool for preparing local cross sections for SEM or TEM (Transmission Electron Microscopy) inspection and analysis. Of the surface analysis methods, AES, as a natural complement and extension of SEM/EDX, has been bought by many wafer fabs and dynamic SIMS is available for dopant and trace analysis. Obviously, the selection of analytical techniques in PFA sections is dependent upon the specific process and product requirements, the availability of external analytical services, and to some degree, the company expertise and "philosophy" in the application of analytical methods.

3. Analytical tasks in a wafer fab

The analytical tasks in a microelectronics manufacturing plant can be grouped into the following categories:

1. *Support for process or equipment ramp-up*:
A new manufacturing process, new (or modified) process steps, or a new piece of equipment may have to be optimised or assessed with respect to an equivalent process. For thin film deposition techniques, (non-directional) plasma and wet etching, cleaning, and ion implantation blanket wafers (i.e. non-patterned wafers) can usually be provided for reliable analytical characterisation. Thus, all of the surface and thin film analytical methods mentioned in the introduction can be applied without lateral resolution restrictions. Of course, questions related to the patterning processes and equipment may need submicron spatial resolution.

2. *Process monitoring*:
Dummy or patterned wafers are regularly pulled from the operating process line after certain process steps. By analysing these wafers it is possible to assertain whether the process steps are still running within the accepted process windows or if corrections are required. Process monitoring is basically a preventive measure, but may also be triggered by a suspected misprocessing. Analytical confirmation of misprocessing can cause the remaining lot to be reworked or, in severe cases, scrapped.

3. *Yield enhancement and defect reduction*:
Defects, wet etch / cleaning, drying stains or small particles of the order of a micron or smaller can render chips electrically irrepairable and so their sources need to be identified and eliminated in order to enhance the production yield of usable dies per wafer. Patterned wafers are thus routinely monitored with respect to their localised defects after certain process steps. Defect inspection tools in the production line generate wafer maps with listings of the optical appearance, position and size of all (or a proportion) of the local defects that were found. Such wafers with their defect maps (e.g. in the form of KLA™ or equivalent files) may then be transferred to an analytical laboratory for physical failure analysis. Here some of the defects are analysed to ultimately determine their route cause. This then allows process engineers to modify the process recipe or tool hardware to eliminate them in the future.

4. *Cause identification of failed devices ("failure analysis")*:
If fully processed ICs or packaged devices fail during electrical test, it is necessary to determine the root cause of the failure in PFA. After electrical identification and localisation of the failure, the device may need decapsulation and deprocessing. This procedure is termed "reverse engineering". The layers of the device need to be removed one by one until the fault can be identified either by microscopy or by elemental analysis.

In the following sections we give a few examples of tasks in which surface analytical techniques were found superior to the more conventional techniques. In order to avoid disclosure of company sensitive process recipes, the accompanying information is restricted to that needed to understand the respective analytical situations.

4. Analytical examples

4.1 Failure analysis of an electrical short

The first example deals with the identification of a "particle" that had caused an electical short in the device (figure 1). Point X-ray spectra were recorded with the SEM/EDX on the particle between the two aluminium tracks and for comparison in a similar space where no particle existed. The two X-ray spectra are almost identical (figure 2), so it was not possible to identify the source of the particle. Therefore, the sample was then analysed in a Field Emission AES (FE-SAM) and, indeed, the Auger spectra (Figure 3) of the corresponding areas gave a clear indication of the particle containing titanium (Ti). Even though a small Ti signal was seen on the "good" area, the Ti peaks from the particle were much more pronounced. Thus it was concluded that the "particle" consisted of a local residue of the Ti/TiN diffusion barrier layer underneath the Al lines. A schematic of the local structure after deprocessing is shown in figure 4. From this it is clear that the analytical resolution of both techniques is limited by scattering effects. In the case of SEM/EDX X-rays are emitted from the entire electron interaction volume underneath and beside the particle, especially including the volume of the Ti/TiN layers within the neighboring Al tracks. It appears that the Ti Kα intensity from these sources is larger than that directly excited by the primary electrons. In the case of AES, Auger electrons can only escape from the outermost monolayers of the solid, i.e. from the narrow sidewalls of the Ti/TiN double layer (< 50 nm thick) but not from its bulk. Thus, the stray signal effect is considerably smaller in AES compared to EDX. Hence, FE-AES has a better "analytical resolution" than the SEM/EDX, despite the electron beam diameter of the FE-SEM being considerably smaller than the one of the FE-AES. This property is the main reason for the application of AES instruments in a semiconductor manufacturing environment.

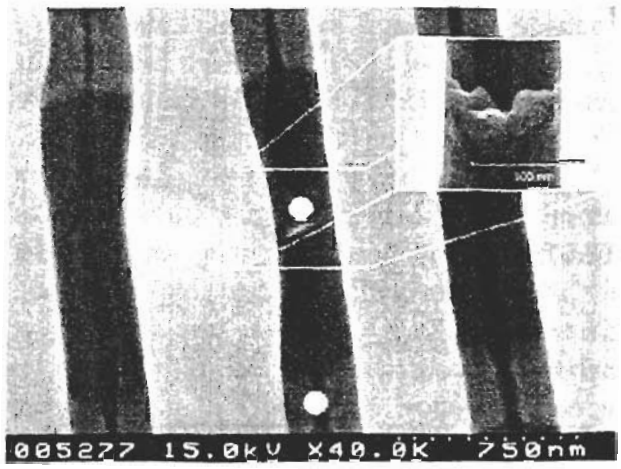


Fig. 1: SEM image of local electrical short between aluminium-based tracks

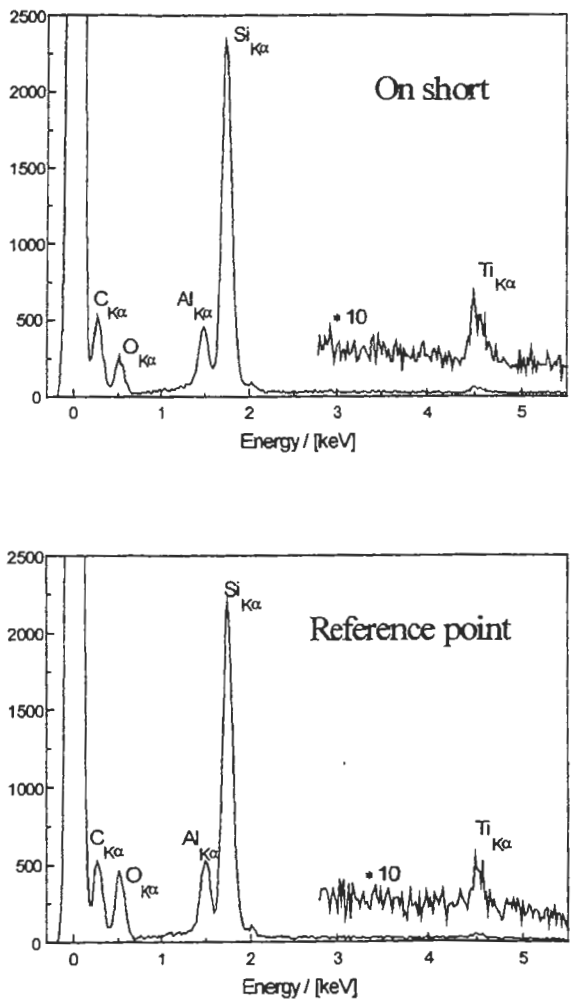


Fig. 2 : 15 keV EDX analyses on the short (top) and on a reference point in the vicinity of the defect (bottom).

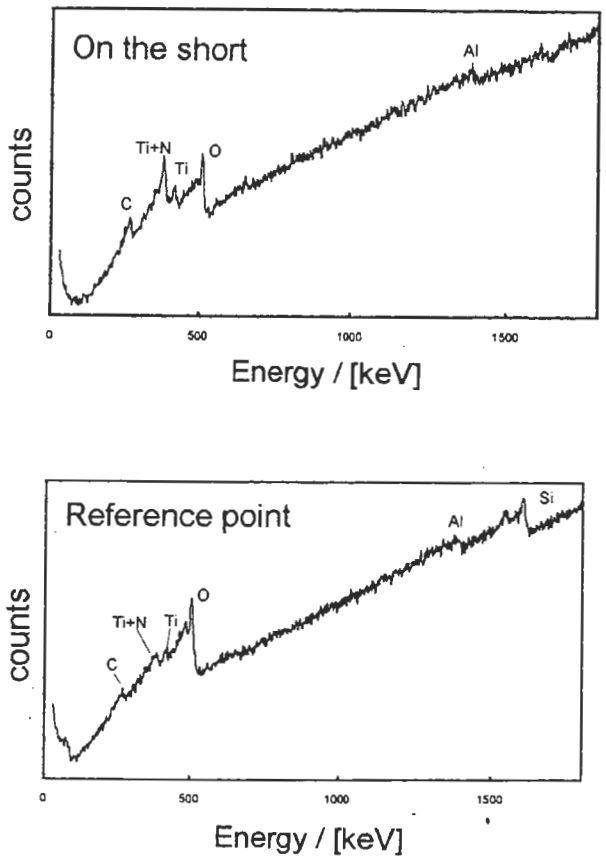


Fig. 3: 10 keV AES analyses on the short (top) compared to the reference point (bottom)

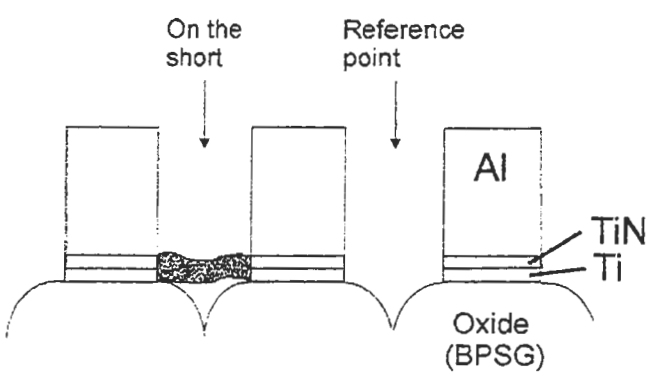


Fig. 4: Schematic of the analytical situation (Not drawn to scale). Line width about 300 nm.

4.2 Particle Analysis

Routine patterned wafer inspection after an integrated gate stack process revealed particles on the surface including a number of unusual "spider-shaped" features (fig. 5). The size of the feature makes it what is termed a "killer defect" as wherever they are formed the die will be rendered electrically irrepairable. In the process doped polysilicon is first deposited on a sub-10 nm thick layer of silicon dioxide and then, in a separate part of the same tool, this layer is coated with tungsten silicide. A FIB cross section was prepared through the defect centre in order to get analytical access to the core. Auger mapping of silicon and tungsten (fig. 6) in a FE-AES (PHI 680) proved the core of the defect consisted of silicon, onto which the tungsten silicide had been chemical-vapour deposited. Thus the cause of the defect could be traced back to the polysilicon deposition process prior to the WSi_X deposition. The spider legs were a consequence of a preferential nucleation and growth phenomenon in the polysilicon process.

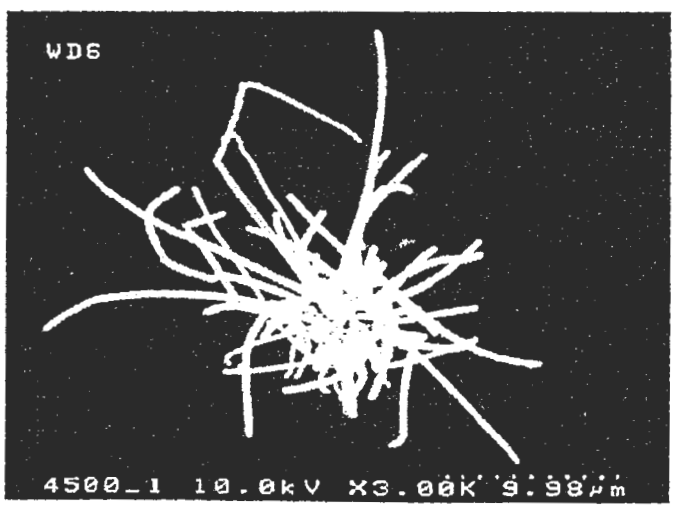
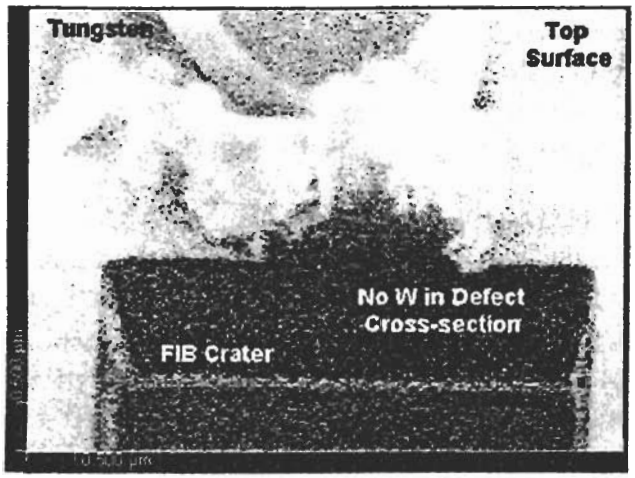


Fig. 5: "Spider" defect on a wafer surface (SEM)



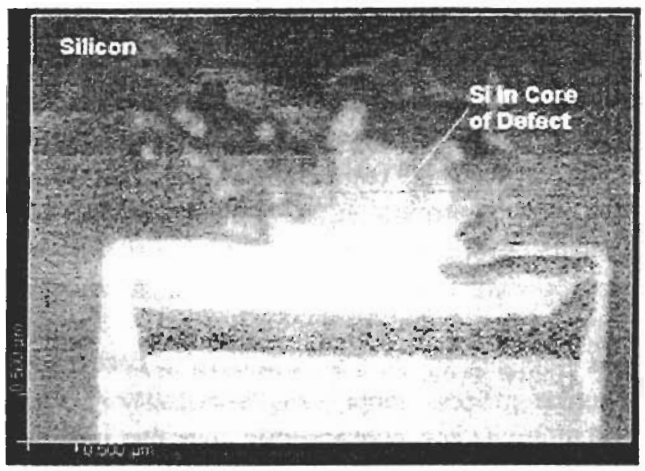
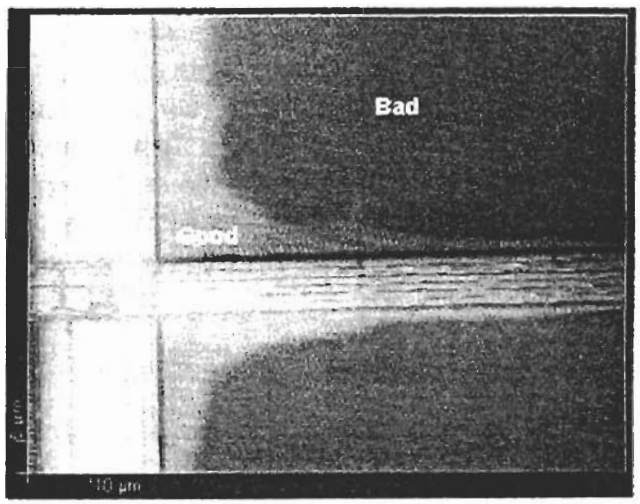


Fig. 6: Auger elemental maps of tungsten (top) and silicon (bottom) of the "spider" defect, recorded on a FIB cross section

Again, the superior analytical resolution of AES (compared to SEM/EDX) provided this unambiguous result. Many other examples of successful particle analyses have been encountered, with particle core sizes even below 100 nm.

4.3 Process monitoring: thin film identification

For process monitoring a wafer was pulled from the middle of the production process after a wet-chemical silicon nitride strip process. To the naked eye, and also in the SEM at low magnification (figure 7), several large discolored areas could be seen on the wafer, suggesting locally incomplete nitride stripping. Top down AES spectra showed only silicon dioxide on both the good and bad areas. Hence, a FIB section was cut through the bad area and analysed by Auger elemental mapping. As is seen in fig. 7 , the nitrogen elemental map shows clearly that the (laterally patterned) nitride layer is still present underneath a surface oxide in the bad areas. Thus it became clear that the wet etch, designed to remove the silicon nitride, had failed due to another silicon dioxide layer on top. Tracing back through the process, it was possible to determine locally incomplete chemical- mechanical polishing of the oxide overlayer as the root cause for this



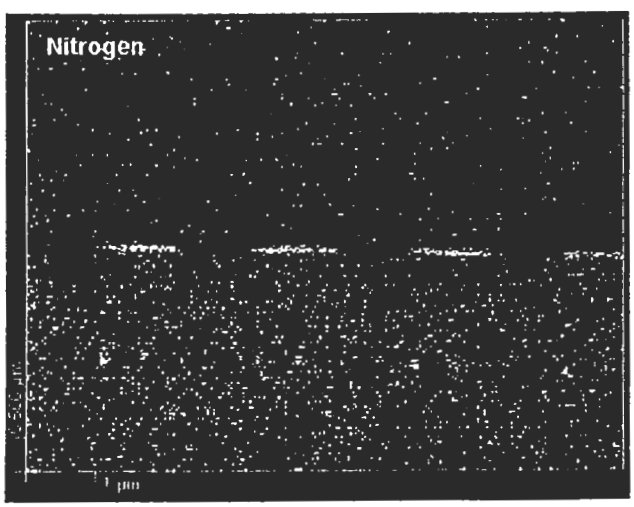


Fig. 7: Top-down SEM image (top) of the wafer and nitrogen Auger map of a 30° tilted FIB section through a "bad" area (bottom)

failure. Obviously, in this type of analysis the AES lateral resolution together with its sensitivity to low atomic number elements (in

this case nitrogen) has been vital to the problem diagnosis. Again, SEM/EDX could not have supplied this result.

4.4 Failure analysis on local trace impurities

After an experimental treatment, an MOS device had failed when operated at elevated temperatures[2]. From the electrical characteristics, contamination by "mobile" ions, predominantly sodium, was suspected but it needed to be analytically confirmed. Due to the extremely low concentration levels that might be involved, the only applicable method was dynamic SIMS. A SIMS depth profile was thus acquired on a "bad" area (hot spot) and compared with the one from a "good" area (Cameca ims 4f, Cs beam, 60 microns diameter of measured area, negative secondary ions to permit improved surface charge compensation)

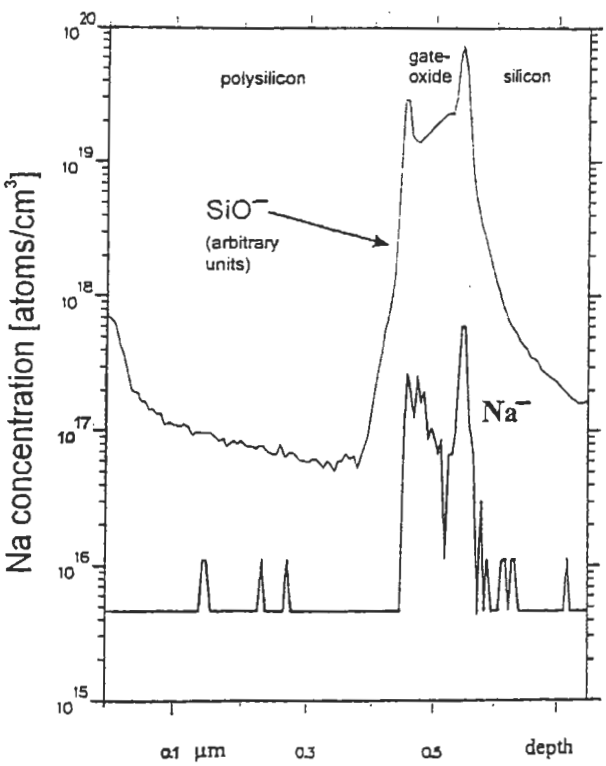


Fig. 8: dSIMS depth profile of sodium recorded from within a failed area of an IC

Indeed, in a certain depth regime, at and between the (oxide-induced) maxima in the SiO^- profile, sodium showed an increase in the intensity but was absent on the "good" area of the sample, thus proving the suspected sodium contamination within the device. In a real process failure situation, further SIMS measurements would help to identify the source of this contamination and to eliminate it.

5. Conclusions

Of the surface analytical methods primarily FE-AES and dynamic SIMS have attained high importance for microelectronics production plants. This is due to the extra analytical information that they offer in comparison to more conventional methods, e.g. SEM/EDX. TOF-SIMS with its surface sensitivity and organic analysis capability has a lot of potential uses in wafer fabs, but has yet to realise full acceptance throughout the semiconductor industry. The largest drawback to the use of surface analysis techniques in the routine process monitoring environment is their low sample throughput and thus the difficulty in getting statistically significant sets of data. The techniques definitely require further development to permit their use in the more routine process monitoring applications. The reliability of the components, thus the uptime of the instruments, the ease of operation (also for non-expert personnel), the time required per analysis, and the degree of automation (in sample handling and in instrumental adjustments) all need to be improved. The complexity of data processing and the lack of reliable automated evaluation routines is also an obstacle to be overcome in the future.

6. Acknowledgement

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7. References

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